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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,069	07/29/2003	Shunpei Yamazaki	0553-0166.01	6156

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EXAMINER	
ABRAHAM, FETSUM	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/629,069	YAMAZAKI ET AL.
	Examiner	Art Unit
	Fetsum Abraham	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-50* is/are pending in the application.

4a) Of the above claim(s) *43-50* is/are withdrawn from consideration.

5)☐ Claim(s) *36-38* is/are allowed.

6)☐ Claim(s) *39-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

As a preliminary matter, the newly introduced device claims 43-50 have been withdrawn from consideration as not directed to the elected claims by original presentation. This application has been subjected to restriction requirement in which the applicant elected method claims in 12/27/04 canceling all device claims. In view of the election, the method claims only have been processed. Please contact the examiner immediately upon receipt of this action for more clarification if necessary and another restriction requirement will be imposed if the applicant does not agree with this action. The device claims, however, are withdrawn at this point of examination and the method claims examined in order to save time with the expectation that the withdrawn claims are acceptable to the applicant.

Please note that the new device claims are qualitatively different in structure and content from the method claims under current examination. They clearly belong to a different class. In view of such an observation and consistent with the election, the examiner suggests that the applicant accepts the withdrawal of the claims in respect of time and correct examination concept.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 39,42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aya et al (6,281,057) in view of Shinada et al (4,597,824).

The primary reference discloses a pixel matrix applicable in display devices and specifically LCDs composed of a pixel portion driver (24) and a gate portion driver (25) formed on common substrate, the remaining structure formed by the method of:

a) Forming an active layer (3) n a substrate, the active layer being an SOI layer,

b) Forming a gate insulation layer (6) on the active layer (see figure 27)

c) Forming a gate electrode (8) on the gate insulation layer using a mask,

d) Forming an impurity implant through the gate.

The prior art discloses all subject matter claimed but may have omitted to user a tungsten gate wiring and the wiring used as a mask in the implantation process of forming the impurities in the active layer. However shinada et al disclose the missing elements in the process. In figure 8, the prior art shows a MOSFET with a gate electrode (114) and a tungsten gate wiring (117) and both elements used as a mask to form impurity regions (118). Therefore, it would have been obvious to one skilled in the art to use a tungsten wiring on gate electrodes specially if the electrodes silicon based materials, since tungsten is known for reacting well with such materials in the formation of dependable silicide layers that provide smooth resistance transition from silicon based gate electrodes to metals by relatively cheaper processing costs.

As for claim 42, sputtering is the most basic method of depositing a metal layer on silicon based layers and would have been obvious to one skilled in the art to use it in the making of the gate layer of the prior art since it has a better focusing feature on a target than vacuum evaporation based processes.

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aya et al (6,281,057) in view of Shinada et al (4,597,824) and further in view of Ono et al (5,422,209).

The first two references may have been silent on nitride interlayer on semiconductor structures formed by the claimed process. However, Ono et al teach on interlayer structures made from a nitride film by plasma CVD processing means. Therefore, it would have been obvious to use nitrides made by the taught process, since the prior art teach that such materials provide excellent adhesion and formability compared to other conventional materials such as amorphous nitrides and oxides (see column 8, 60-65).

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aya et al (6,281,057) in view of Shined et al (4,597,824) and further in view of Tanabe et al (6,503,819).

The first two references may have also been silent on a laminated gate structure composed of tungsten and tungsten nitride films. However, Tanabe et al teach on the subject matter in claim 16. Therefore, it would have been obvious to one skilled in the art to use a multilayered gate structure composed of tungsten and tungsten nitride films, since the first provides the advantage mentioned above and tungsten nitride blends well with tungsten and silicon based materials and provides a specific advantage in serving a barrier layer that protects metal diffusion to the silicon layer or the vise versa at high processing temperatures.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Refer to PN: 6,531,713 where LDDs in driving circuits have more impurity concentration than those in pixel circuits.

Claims 36-38 have been allowed.

Although structures with tungsten gate wiring as in (4,985,740) and a gate formed by using resist mask and implanting active regions in a layer using a resist mask as in (6,281,057) have been known in the past, a composite structure whereby a gate electrode is provided with tungsten gate wiring over the gate electrode using a resist mask and forming an impurity regions in a substrate using the gate wiring and the resist that was used in the making of the wiring as a mask is not taught or rendered obvious by the prior arts.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham
7/5/05